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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,993	11/02/2001	Gibong Jeong	TI-33192	1296
23494	7590	04/05/2005		EXAMINER
				PERILLA, JASON M
			ART UNIT	PAPER NUMBER
			2634	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/052,993	JEONG, GIBONG
	Examiner Jason M Perilla	Art Unit 2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 02 November 2001.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,3,5-8 and 20-23 is/are rejected.
- 7) Claim(s) 2,4 and 9-19 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 02 November 2001 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/02/01</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. Claims 1-23 are pending in the instant application.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on November 2, 2001 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: figure 1, reference 118. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 1-19 are objected to because of the following informalities:

Regarding claim 1, in lines 3-4, "the gain and phase imbalance" is lacking antecedent basis.

Regarding claim 2, the variables γ and β_Q are not defined in the claim. In lines 1-2, "the gain mismatch" is lacking antecedent basis, in line 3, "the real and imaginary components" is lacking antecedent basis, and, in line 5, "a IQ-swapped spreading sequence" should be replaced by –an I/Q-swapped spreading sequence--.

Regarding claim 4, in lines 1-2, "the phase mismatch" is lacking antecedent basis.

Regarding claim 9, in lines 1-2, "the phase mismatch" is lacking antecedent basis.

Regarding claim 10, the meaning of the function $X(\gamma, \theta)$ is not defined in the claim such that one could appropriately use it, and the variables γ and θ are not defined in the claim such that the function $X(\gamma, \theta)$ could be evaluated. The variables γ and θ in claim 10 are not assumed to be defined in a parent claim because they are not designated by a "carrot".

Regarding claim 11, in line 1, "the gain and phase imbalance" is lacking antecedent basis.

Regarding claim 12, the claim is objected to for the same reasons as applied to claim 10 above.

Regarding claim 13, in line 1, "the gain and phase" should be replaced by –the gain and phase imbalance--.

Regarding claim 14, in lines 3-4, "the real component" and "the imaginary component" are each lacking antecedent basis, in line 6, the despread pilot signal is lacking antecedent basis, and, it is suggested by the Examiner that lines 6-7 are replaced by "finding the difference between the real component of the pilot signal despread by the normal spreading sequence and the imaginary component of the pilot signal despread by the IQ-swapped spreading sequence."

Regarding claim 17, the claim is objected to for the same reasons as applied to claim 14 above.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 3, 5, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Glas (US 6330290).

Regarding claim 1, Glas discloses by figure 1 a digital baseband circuit, comprising: first and second input ports (I1' and Q1') for receiving digital input signals from analog to digital converters (27 and 27'); a controller (56) coupled to the first and

second input for estimating the gain and phase imbalance of the digital input signals (col. 1, line 25 – col. 2, line 8).

Regarding claim 3, Glas discloses the limitations of claim 1 as applied above. Further, Glas discloses that the controller comprises a digital signal processor or DSP (fig. 1, ref. 56).

Regarding claim 5, Glas discloses the limitations of claim 2 as applied above. Further, Glas discloses a gain and phase correction circuit (fig. 1, refs. 40, 42, 44, and 48) coupled to the first and second input ports.

Regarding claim 6, Glas discloses the limitations of claim 5 as applied above. Further, Glas discloses by figure 1 that the gain and phase correction circuit includes first (40) and second (44) multipliers coupled to the first input port and third (42) and fourth (48) multipliers coupled to the second input port.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 7, 8 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glas in view of Lewis (US 4489392).

Regarding claim 7, Glas discloses the limitations of claim 6 as applied above. Glas discloses that the digital signal processor is coupled to the first, second, third, and forth multipliers as illustrated in figure 1. Further, one skilled in the art is aware that a

digital signal processor may utilize any number of methods to create the phase and gain outputs illustrated. However, Glas does not explicitly disclose that a look up table is coupled to the phase and gain correction circuit to supply the phase and gain correction signals. However, Lewis teaches a method of phase and gain correction for quadrature signals wherein a look up table (fig. 2, ref. 59) is utilized to create a phase/gain signal to a multiplier (fig. 2, ref. 51; col. 2, lines 33-36, 50-55). One skilled in the art is aware that the digital signal processor could, alternatively, create the phase and gain output signals using an internal lookup table or, as taught by Lewis, an external memory lookup table because the creation of the phase and gain output signals according to a lookup table is easy to implement and effective. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a lookup table as taught by Lewis in the phase/gain correction circuit of Glas because it could be used to easily and effectively create the phase and gain correction signals to be applied to each of the multipliers of the correction circuit.

Regarding claim 8, Glas in view of Lewis disclose the limitations of claim 7 as applied above. Further, Lewis discloses that the lookup table is implemented as a read only memory (col. 2, lines 33-36).

Regarding claims 20 and 21, the limitations of the claims are met applied as claims 7 and 8 above. It is noted that, in the apparatus of Glas in view of Lewis, the read only memory lookup table supplies each of the multipliers with a separate gain or phase correction signal.

Regarding claim 22, Glas in view of Lewis disclose the limitations of claim 20 as applied above. Further, Glas discloses by figure 1 a fifth multiplier (52) having a first input port for receiving an output from said first multiplier (40) and a second input port for receiving an output from said second multiplier (48), and having an output port for providing a corrected I signal (I2); and a sixth multiplier (54) having a first input port for receiving an output from said third multiplier (44) and a second input port for receiving an output from said fourth multiplier (42), and having an output port (Q2) for providing a corrected Q signal. It is noted by the Examiner that the multipliers (52 and 54) are considered multipliers at least as much as those shown in the illustration of the claimed embodiment of the instant application according to figure 2, references 210 and 212.

Regarding claim 23, Glas in view of Lewis disclose the limitations of claim 22 as applied above. Further, the I and Q signals are necessarily digital signals as illustrated by Glas in figure 1 because they are converted into digital by the analog to digital converters 27 and 27'.

Allowable Subject Matter

9. Claims 2, 4, 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
10. The indication of allowable subject matter is made regarding claims 11-19.
11. The following is a statement of reasons for the indication of allowable subject matter:

Claims 2, 4, and 9-19 are indicated to contain allowable subject matter because the prior art of record does not disclose or obviate the identification of a gain/phase imbalance from a received despread complex signal (having I and Q components) wherein a first of the two received despread signals is despread by a normal locally generated spread sequence, and the second of the two received despread signals is despread by an I/Q swapped locally generated spread sequence to identify the imbalance.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record not relied upon above is cited to further show the state of the art with respect to gain and phase balancing circuits.

U.S. Pub. No. 2003/0135532 to Peting.

U.S. Pat. No. 6574286 to McVey.

U.S. Pat. No. 6442217 to Cochran.

U.S. Pat. No. 5705949 to Aleyunas et al.

U.S. Pat. No. 5412351 to Nystrom et al.

U.S. Pat. No. 4876489 to Cawthorne.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

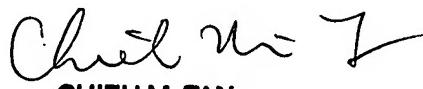
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jason M. Perilla
March 31, 2005

jmp



CHIEH M. FAN
PRIMARY EXAMINER